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For

Radiation Sensing Integrated Circuit Device and Method

by

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RADIATION SENSING INTEGRATED CIRCUIT DEVICE AND METHOD

BACKGROUND OF INVENTION

RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/224625, filed August 11, 2000, and entitled "RADIATION SENSING INTEGRATED CIRCUIT DEVICE AND METHOD". This provisional application is incorporated herein by reference.

1. Field of the Invention

The present invention relates generally to the field of sensing devices, their use and methods for their manufacture, and more particularly, to a radiation sensing integrated circuit for positional purposes. The device and method is particularly well suited for use in navigation, guidance and control systems, for example systems in space or used for space exploration, or other systems including positional control of systems relative to incoming radiation.

2. Technical Background

Light (radiation) inherently contains direction and amplitude characteristics. Consequently, light (radiation) is useful in navigational and positional control applications. For example, sensors have been developed for use in vehicle guidance and control systems allowing navigation of vehicles relative to a light (radiation) source.

Positioning sensors that function in response to incident radiation are known in the art. One example of a guidance or a positioning system that uses a light or radiation source such as the sun for positioning is known in the art as a sun pointer. One such existing sun pointer system employs electro-optical sensing devices in conjunction with

some type of mechanical alignment to guide the impinging light or radiation relative to the electro-optical sensors. **FIG. 1** illustrates a sun pointer system **100** that employs such a design. The sensing element of system **100** is a photodiode array **106**. Light (radiation) impinges the array **106** through a mechanical entrance slit **104**, providing direction and amplitude information to the system. Typical pointing systems of this type weigh approximately a quarter of a pound and require an input power of .25 to 1.0 watt.

U.S. Patent No. 4,611,914, entitled Sunbeam Incident Angle Detecting Device, illustrates a sun pointer system for determining position relative to a light source. The technology disclosed in the '914 patent uses a pair of solar cells disposed perpendicular to each other. When radiation impinges, the current produced by the radiation in the solar cells is used to determine the incident angle of the radiation. This angle is then used to determine the relative position of a satellite to a light source.

The existing technology for determining the position using the angle of incidence of radiation has several disadvantages. The optical systems currently in use are large, heavy, and require a significant amount of space to perform the sensing function required by the pointing system. In addition, sun pointers in the prior art require significant power.

What is needed, but currently unavailable in the art, is an improved radiation sensing device that is small in size, capable of accurately providing information relating to directional position, light weight, and which has minimal power requirements for its use and operation. Such a device should be simple to use, easily adapted for use with existing equipment, and inexpensive to manufacture. It is to the provision of such a device that the present invention is primarily directed.

SUMMARY OF THE INVENTION

One aspect of the present invention is a system and method for determining the azimuth and elevation of radiation impinging the surface of an Integrated Circuit ("IC"). In order to determine azimuth and elevation of impinging radiation, a sensor detects the angle of incidence of impinging light (radiation) in both an x-plane and a y-plane. These rectangular coordinate outputs of the sensors can then be translated into spherical coordinates electronically as required. The angle of incidence information for the two planes provides the complete azimuth and elevation information.

Another aspect of the present invention is a silicon based directionally sensitive radiation sensor differential pair ("VCELL") fabricated using essentially conventional monolithic integrated circuit ("IC") technologies. The sensor of the present invention is constructed on a standard silicon wafer. Differential pairs are formed on the surface of the integrated circuit such that the angle of incidence of impinging radiation can be detected in both an x-plane and a y-plane. The differential pair consists of two NPN phototransistors formed in the <100> plane each having a P type base region or base extension formed in the <111> plane of the silicon. The <100> and <111> P type base regions are formed in a converging manner at a 54.7° angle.

Yet another aspect of the present invention relates to a system that determines the azimuth and elevation of radiation that is impinging the IC device of the present invention. The system includes the IC device described, infra, that detects the angle of incident of the impinging radiation in both an x-plane and a y-plane. The system further includes a circuit that performs calculations on the angle of incidence information detected by the integrated circuit to determine the azimuth and elevation of the impinging radiation.

Another aspect of the present invention is an IC as described, infra, having two VCELL structures and a reference transistor. The reference transistor is a phototransistor formed in the <100> plane of the silicon chip. The reference transistor detects impinging radiation to provide a normalization amplitude (or reference) value. Therefore, when calculating the angle of incidence of the radiation, the signals from each transistor of a

single differential pair (VCELL) are subtracted. The difference (the differential output of a single VCELL structure) is divided (normalized) by the output of the reference transistor thus removing radiation amplitude from the final signal outputs of the sensor when computing azimuth and elevation.

The device, system, and method of the present invention allow for the miniaturization of radiation sensing. The miniaturized sensor of the present invention allows for the accurate determination of direction and position of an object relative to a known source of radiation. Further, the present invention provides a small, lightweight, rugged, low power and inexpensive device to be employed in vehicles or systems where size, weight and power are a factor such as vehicles for space applications. In addition, the miniature sensor may be used to detect increased solar radiation to reconfigure shielding on spacecraft during solar flares and storms. The sensor may also be used to prevent the inadvertent pointing of sensitive optical systems, such as in telescopes, at bright sources of radiation that might cause damage

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of the specification, illustrate embodiments of the invention, and, together with the description, serve to explain the principles of the invention:

FIG. 1 (prior art) is a device employing a mechanical slit and electro-optical sensors in order to obtain the angle of incidence of impinging radiation.

FIG. 2 is a block diagram describing the functionality of the sensor integrated circuit and further including its relationship to a computational device or circuit.

FIG. 3 is a cross-sectional view of the typical VCELL structure of the present invention illustrating two <100> bipolar junction phototransistors with opposing <111> base extensions (offset from each other by opposing <111> planes or an angle of 70.6 degrees).

FIG. 4 is a circuit diagram modeling the VCELL structure of the present invention.

FIG. 5 is a circuit diagram modeling the dual-axes VCELL structure of the present invention.

FIG. 6A & 6B are graphs indicating the first order current behavior of the phototransistors of the IC.

FIG. 7 is a diagram of an IC of the present invention illustrating three VCELL structures, a reference transistor, some additional test structures, interconnect metallization and bond pads.

FIG. 8 is a diagram illustrating a topological view of a VCELL structure of the present invention (not drawn to scale).

FIGS. 9A-9D are successive topological views of the VCELL structure through the masking process steps during formation.

FIGS. 10A-10H illustrate cross-sectional views taken along line A-A in **FIG. 9**, of successive process steps for making a VCELL of the present invention.

FIG. 10I is a cross-sectional view, taken along line A'-A' in **FIG. 9A.**

FIG. 11 is a block diagram illustrating a system of the present invention having two separate and independent detector structures, the outputs of which are used to calculate azimuth and elevation of impinging radiation.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numerals will be used throughout the drawing figures to refer to the same or like parts. An exemplary embodiment of the present invention is a silicon based integrated circuit ("IC") capable of detecting light (radiation). An exemplary embodiment of the integrated circuit that detects radiation is described functionally in the block diagram in **FIG. 2**, and is designated generally throughout as reference numeral **116**.

The IC **116** includes an x-axis detector **118** capable of detecting the angle of incidence in an x-plane of impinging radiation, a y-axis detector capable of detecting the angle of incidence in a y-plane, and a reference detector. The x-axis and the y-axis

detectors, **118** and **120,** have dual outputs that are amplified photocurrents caused in the detectors by the impinging radiation. The x-axis detector **118** has output currents I_{x1} and I_{x2}. The y-axis detector **120** has output currents I_{y1} and I_{y2}. The reference detector is a phototransistor formed in the <100> plane of the silicon. The reference detector is designed to provide a normalization current, I_{ref}, to factor out the amplitude of radiation impinging the surface of the IC. The net amplified generation recombination photocurrent produced in the x-axis detector **118** is I_x where

$$I_X = I_{X1} - I_{X2}$$

Therefore, I_x is the differential output of the x-axis detector **118**. The normalized photocurrent output of the x-axis detector **118** is given by dividing the above by I_{ref} giving

$$I_X / I_{ref} = [I_{X1} - I_{X2}] / I_{ref}$$

The photocurrents produced in the y-axis detector are denoted as I_{y1} and I_{y2} The net generation recombination photocurrent produced in the y-axis detector is I_y where

$$I_Y = I_{Y1} - I_{Y2}$$

Therefore, I_y is the differential output of the y-axis detector **120**. Dividing by Iref, the same as in **118**, normalizes the outputs.

A preferred embodiment of the IC **116** can include two directionally sensitive radiation sensors or differential pairs ("VCELL") that are disclosed, supra. A VCELL device is used in the IC **116** as the x-axis detector **118** (**FIG. 2**), and a VCELL device is used as the y-axis detector **120** (**FIG. 2**). A VCELL device detects the radiation in only one axis. Therefore, in order to detect an x-plane and y-plane direction, two VCELLS are formed on the IC surface.

A VCELL of the present invention is illustrated in **FIG. 3** and is designated generally throughout as reference numeral **126**. **FIG. 3** is a cross-sectional view of a single VCELL device **126** that is formed as a conventional monolithic IC. The VCELL

includes two identical, yet opposing, phototransistors **128** and **130**, formed in the silicon wafer. Generally, the phototransistors are formed in the silicon substrate **142** in the <100> plane **132.** The <111> plane **134** is the silicon plane that is at an angle of 54.7 degrees from the <100> plane **132**. The phototransistors **128** and **130** are formed in the surface of the chip, primarily in the <100> plane, but with a base region extension down the <111> plane **140** such that the P type base regions **140** in the <111> plane **134** are formed opposing and convergent with the <100> base regions **138**. The structure formed is a v-groove **129** having a <100> plane horizontal structure **127** at the most convergent point (bottom) of the v-groove.

Each phototransistor **128** and **130** is a bipolar junction transistor having two rectifying PN junctions formed from extrinsic semiconductor materials of the P type and the N type. The phototransistors are NPN transistors. The transistors **128** and **130** are formed on an N type silicon substrate **142**. The silicon substrate forms the collector of each phototransistor, **128** and **130**. In addition, the phototransistors include a P type base that includes a P type base region **138** in the <100> plane **132** and a P type base region **140** in the<111> plane **134**. The emitters **136** are heavily doped N type and are formed in the <100> plane, **132**.

The phototransistors **128** and **130** that form the VCELL device **126** also include a silicon dioxide (SiO_2) layer **146** and an interconnect layer **144** consistent with standard silicon planar process technology. The interconnect layer **144** is typically aluminum, or aluminum with a small amount of silicon (typically 1-2%), deposited as a thin film layer on the chip. The introduction of silicon in the aluminum interconnect layer **144** minimizes surface pitting by the aluminum during processing. A second important role for the interconnect layer is that it is designed to minimize the generation of photocurrents in **128** and **130** in the <100> plane **132** when the surface of the chip is exposed to impinging radiation.

The phototransistors **128** and **130** of the VCELL device **126** detect impinging radiation. The impinging radiation is received, at an angle of incidence relative to the

IC's surface or the <100> plane, on the <111> P type bases **140**. The impinging radiation creates a photocurrent in the PN junction of the P type base **140** and the N type substrate **142**. In essence, this PN junction behaves like a photodiode, and it can be modeled as such, providing a photocurrent into the <100> base **138** that is subsequently amplified by the transistor.

The VCELL device as shown in **FIG. 3** is modeled by the equivalent circuit in **FIG. 4.** The schematic equivalent of the single axis VCELL is designated generally throughout as reference numeral **148**. A voltage source V_{CC} **150** provides voltage to the device and by design is the voltage applied to the IC substrate **142**. This voltage source can be of a type known to those skilled in the art. The circuit diagram of the single axis VCELL detector includes emitters **164** and **166** corresponding to the N type heavily doped silicon emitters **136 (FIG. 3)**. The collector regions **160** and **162** correspond to the N type silicon substrate **142 (FIG. 3)**. In addition, the base terminals **168** and **170** of the VCELL **148** correspond to the P type silicon bases both in the <100> plane **132 (FIG. 3)** and the <111> plane **134 (FIG. 3)**. The photocurrent sources **156** and **158** modeled in the circuit diagram represent the photocurrent generated by the absorption of the incident radiation by the PN junction formed between the P type silicon bases in the <111> planes **140** and the n-type substrate **142**. Due to the circuit design, the transistors **152** and **154** behave as amplifiers, amplifying the photocurrents from the current sources **156** and **158.** The PN junction between the P type silicon bases on the <111> planes and the N type silicon substrate are modeled in the circuit by diodes **149** and **151**. The model current sources **156** and **158** are connected between the transistor bases **168** and **170** and the transistor collectors **160** and **162** shown in **FIG. 4**. Additional bias voltages can be applied to the transistors **152** and **154** at their base and emitter terminals **168, 164, 166** and **170, as** required, by those skilled in the art.

FIG. 4 is a schematic drawing of a single axis VCELL. A single VCELL can only detect a single directional dimension of the impinging radiation. Two VCELL devices are required to detect a second directional dimension of the same impinging radiation. **FIG. 5** models the dual VCELL device required to receive both a first and

second directional dimension of impinging radiation on an IC surface. Dual axes detector **172** includes two VCELL devices **174** and **176**. The VCELL devices must be arranged on the chip surface so that the devices sense different dimensions of the impinging radiation. Different dimensions can be defined by an x-axis directional dimension and a y-axis directional dimension. Physically, the VCELL detectors must be arranged nonparallel. For example, if the VCELL detectors were arranged parallel, then the devices would receive radiation in the same directional dimension, thereby only detecting a single rectangular coordinate value in a single dimension. To completely determine the angle of elevation and azimuth of the incident radiation, two independent directional measurements are required at different angles to the incoming radiation. This allows calculation of the azimuth and elevation of radiation impinging the surface of the IC.

In general, it is not necessary that the two chosen directional dimensions, X and Y be orthogonal. In the present embodiment, in order to take process advantage of the relationship between the <100> axis and the <111> axis of single crystalline silicon, the X and the Y axes orientation are orthogonal in this embodiment.

The PN junction of the N type substrate **142** and the P type base **140** in the <111> plane is modeled in the circuit schematic photodiodes **178, 180, 182,** and **184 (Fig. 5)**. The photocurrent I_P, produced in a PN junction is expressed as a function of the angle of incidence of the radiation, θ, by the following equation

$$I_P = A * \sin\theta$$

If scattering effects (and any other second order effects such as shadowing by surface objects at very small angles of incidence) are neglected, A is essentially independent of θ. Otherwise, the dependence of A on θ must be taken into account. This fact does not change the generalized analysis and results presented herein in any significant way for angles of incidence greater than typically 1 (one) degree. If phototransistors or photodiodes are fabricated on different planes in the silicon, then the above expression can be modified to give the value of photocurrents in these devices relative any reference. For example, if the reference plane is the <100> plane in silicon **132** (**FIG 3**), then the

equation, including the offset, for the photocurrent produced along the x-axis, in an offset plane, is:

$$I_P = A * \sin(\theta_x \pm \text{offset})$$

The choice of ± in the equation above depends on which opposing plane is chosen.

Assuming the configuration as shown in **FIG. 2**, the device has 3 detectors, an x-axis detector **118**, y-axis detector **120**, and a reference detector **122**. The photocurrents produced in the x-axis detector are I_{px1} and I_{px2}. The resulting current behavior is illustrated in the graph shown in **FIG. 6A**. The reference transistor photocurrent is **188**. The currents in the current sources $I_{px1}$and I_{px2} are indicated by graph lines **186** and **190**. Under the assumption that scattering can be neglected to a first order and also under the assumption that the offset angle is 54.7 degrees (the <111> plane in silicon forms a 54.7 degree angle with the <100> plane), the graph in **FIG. 6A** defines the current behaviors in the detectors. The plots in the graph in **FIG. 6A** are shown normalized.

A reference transistor (or detector) **122** (**FIG.2**) produces a photocurrent, I_{ref}. The normalized output of the x-axis VCELL is thus given by the equation

$$I_{NX} = [\, I_{px1} - I_{px2} \,] / I_{ref}$$

The above equation of normalized output I_{NX} is plotted in **FIG. 6B.**

An alternative normalization can be accomplished by normalizing using the sum of all currents for one axis.

In this alternative case,

$$I'_{NX} = [I_{px1} - I_{px2}] / [I_{px1} + I_{px2} + I_{ref}]$$

This alternative normalization form is useful when a normalized output that varies from +1 to −1 is required over a range of angle of incidence of 0 – 180 degrees. The curvature shown in Fig. 6B can thus be avoided as required.

The normalized output of the y-axis VCELL is:

$$I_{NY} = [\ I_{py1} - I_{py2}\ ] / I_{ref}$$

The equation for the normalized VCELL output signal for the X-axis detector is:

$$I_{NX} = [I_{px1} - I_{px2}] / I_{ref} = [\sin(\theta_x - 54.7°) - \sin(\theta_x + 54.7°)] / \sin\theta_x$$

The equation for the normalized VCELL output signal for the y-axis detector is:

$$I_{NY} = [I_{py1} - I_{py2}] / I_{ref} = [\sin(\theta_y - 54.7°) - \sin(\theta_y + 54.7°)] / \sin\theta_y$$

The above equations are not accurate for angles of incidence less than 1 (one) degrees. In this case surface-shadowing effects must be taken into account.

All of the above-described photocurrents get multiplied by the gain factor (ß+1) of the matched transistors that make up the VCELL detectors and the reference detector. The ß+1 gain factor drops out with normalization. However, in all cases, the actual output of each detector is the emitter currents.

FIG. 11 is a block diagram illustrating a preferred embodiment of the system of the present invention. The system **500** includes an IC **502**, a VCELL processor **504**, and an interface **506**. The IC contains two VCELL detectors, an x-axis detector **508** and a y-axis detector **510**. When radiation is detected photocurrents, I_1 and I_2, are produced in the x-axis detector **508** and photocurrents, I_3 and I_4, are produced in the y-axis detector **510**. The currents produced provide the angle of incidence information of the incoming

radiation for the two planes, θ_X and θ_Y The computational device **504** calculates the azimuth θ_Z, and the elevation, φ by applying the following formulas:

$$\tan \theta_Z = \tan \theta_X / \tan \theta_Y,$$

and

$$\tan \varphi = \{ [1/\tan^2\theta_X] + [1/\tan^2\theta_Y]\}^{1/2}$$

The computational device **504** and the interface device **506** can be integrated into a single device. Similarly, the interface device may not be used. In addition, the output of the computational device **504** can be either analog or digital as desired. All these options are known to those skilled in the art.

In **FIG. 10A**, silicon substrate **380** suitable for integrated circuit manufacture includes N type silicon with a planar surface, a <100> orientation, and a resistivity of typically 6 ohm-cm. The thickness of the silicon substrate is approximately 14 mils. A Silicon Dioxide (SiO_2) layer **400** is formed on the top surface of substrate **380** having a thickness of approximately 4,000 angstroms.

A layer of photoresist is applied as a continuous layer on the surface of the SiO_2 layer **400** and selectively irradiated using a photolithography system. A first mask is used to implement the selective irradiation, projecting the image as shown in **FIG. 9A**. The first mask delineates the areas that will form the first boron deposition. The photoresist is developed and the irradiated portions are removed to provide the opening **383** (**FIG. 10B**) after a subsequent oxide etch process. All photoresist masking operations use standard photolithography techniques known to those skilled in the art for silicon planar processing technology.

In **FIG. 10C**, photoresist has been stripped, the oxide aperture has been etched and doped P-region **386** is implanted or diffused into substrate **380** by subjecting the structure to ion implantation of boron or by thermal diffusion by subjecting the wafer to high temperature with a source of boron dopant such as boron nitride wafers. The boron

deposition and subsequent diffusion/oxidation forms a P-region with a junction depth of .8-1 micron and a sheet resistance of approximately 300ohm/sq. Oxide layer **388** is grown on the substrate **380**. The oxide layer has a thickness of approximately 2,000 angstroms over the P-region **386**.

A layer of photoresist is applied to the silicon substrate **380**. A second mask is used to implement the selective irradiation, projecting the image as shown in **FIG. 9B**. The second mask delineates the areas which will receive a first silicon etch, a second boron deposition and a second silicon etch. The base **220** remains as previously developed, and the rectangular image **226** is projected onto the surface of the wafer. Thereafter, the photoresist is developed and the irradiated rectangular portion **226** is ready for subsequent processing.

In **FIG. 10D** the v-groove **390** is preferentially etched (the first silicon etch) forming the opposing convergent sidewalls **394** and **392** oriented in the <111> plane. Etching is performed where the <100> plane is etched approximately thirty (30) times faster than the <111> plane using a wet chemical preferential etching solution of KOH, IPA and H_2O at 80 C°. The <111> plane in silicon intersects the <100> plane at an angle of 54.7 degrees. Therefore, the resulting structure is shown with a v-groove having an angular slope from the <100> plane of 54.7 degrees. In addition, the etching separates the boron doped (P type) <100> region **386** (**FIG. 10C**) into two separate and distinct P-type base regions in the <100> plane, **396** and **398**.

In **FIG. 10E** a second doped P type region **400** is implanted into substrate **380** by subjecting the structure to ion implantation of boron or by thermal deposition and diffusion/oxidation with a boron dopant source such as boron nitride wafers. The second Boron deposition forms a P type region in the <111> planes **394** and **392** as well. The second P type regions **394** and **392** have a junction depth of approximately 0.8 – 1.0 microns.

In **FIG. 10F**, a second silicon etch is performed on the v-groove **390** providing additional depth of approximately 1-2 μ (microns). This further etching allows for the separation of the boron-doped P-region **400** leaving only a P type base region **402** on the <111> plane and a P type base region **404** on the opposing <111> plane. The opposing P type base regions on the opposing <111> planes form part of the base regions of the NPN phototransistors.

In **FIG. 10G**, an oxide layer **403** is grown on the bare silicon regions in the v-groove **390**. The oxide layer has a thickness of approximately 2,000 angstroms. This oxidation masks the silicon surfaces such that when masking the surface to apply the N^+ depositions the doping will not penetrate areas other than those to be doped.

A layer of photoresist is applied across the entire wafer. A third mask is used when implementing the selective irradiation, creating the image as shown in **FIG. 9C**. This masking step delineates the regions where the N^+ doped areas **230** and 228 (**FIG. 9C**) are formed. The N^+ regions are formed using either ion implantation or thermal diffusion using a source of phosphorous or arsenic or both. The N^+ regions **230** form the emitters for the bipolar phototransistor. The N^+ regions **228** provide a means of separation between the boron doped P type <111> planes formed in **FIG. 9B** by the end sections of **226**. This provides that the phototransistor devices are conductively isolated from each other. The base **220** remains as previously formed.

With reference to **FIG. 10G**, the photoresist is developed and the irradiated portions are removed providing the openings **406** and **407** for emitters after an oxide etch process.

The heavily doped N^+-regions **408** and **410** are formed in substrate **380** by subjecting the structure to ion implantation or thermal diffusion of phosphorous or arsenic. In addition, with reference to **FIG. 9C**, the end regions of the v-groove **228** are heavily doped in order to terminate the p type <111> base regions (converting the P regions in this area back to N regions). The phosphorous depositions form N^+ regions,

408 and **410**, that serve as the emitters of the phototransistors. The N^+ regions have a junction depth of approximately 1.0-1.5 microns.

With reference to **FIG. 10I**, a layer of photoresist is applied on the silicon and a fourth mask is used to create the contact openings **416** to the P type base regions and to all N type material. The photoresist is selectively irradiated using the photolithography system and the fourth mask, then the irradiated portions are removed to provide a consecutive line of openings to serve as the P type base contacts **416** and provide all contacts to the N type material, including the N^+ emitters.

FIG. 9D illustrates the placement of the P type base contacts **416** along the substrate surface. The consecutive arrangement minimizes the effect of base spreading resistance by reducing the series resistance inherent in the silicon material used in the P type base regions, **402,404, 396 and 398. (FIG. 10F**).

Further processing steps in the fabrication of ICs are known in the art and further include forming an interconnect metallization layer forming contacts to the the P type base regions **416** (**FIG. 10I**) and the N^+ emitters **408** and **410** (**FIG. 10H**), then masking the interconnect metallization pattern to form the interconnects to the bond pads on the chip from the contacts.

Generally, the exemplary embodiment described herein includes an integrated circuit device having three phototransistors including two phototransistors having bipolar junction transistors and a reference phototransistor. One of ordinary skill in the art will recognize that the v-groove structure disclosed that makes up the opposing and convergent P type base regions of the phototransistors can be made using various planes, surfaces and geometric configurations. The present invention is not limited to P-type base regions formed in a <111> plane. In addition, one of ordinary skill in the art will recognize that the choice of bipolar junction phototransistors is also not limiting. Other devices, PNP (as opposed to NPN as described) transistors, MOSFETS, or other types of

devices can be employed to serve the function of the NPN phototransistors in the preferred embodiment.

Also, various methods of processing are available in the art to form other various planes, surfaces or geometric configurations. For example, methods including ion milling, plasma etching, micro-electro-mechanical structuring (MEMS), or micro-machining are available to form various other planes, surfaces and geometric configurations. The present invention is not limited to the crystallographic method described herein. The embodiment disclosed herein is an exemplary embodiment of the present invention.

In addition, the present invention includes other numerous variations available to the embodiment described herein. For instance, the IC can include a single VCELL device or numerous VCELL devices on the surface of the chip depending upon the application required of the IC. In addition, when required, the VCELL structure can be halved such that it is formed using on a single transistor structure thus eliminating the differential transistor structure. The system of the present invention can employ various kinds of devices to perform the calculations required for determining azimuth and elevation, including a microprocessor or a ROM device.

Those skilled in the art will readily implement the steps necessary to provide the structures and methods disclosed herein, and will understand that the device, system and method parameters, materials, and dimensions are given by way of an exemplary embodiment of the present invention. These various parameters, materials, and dimensions can be varied to achieve the desired structure as well as any modifications of the present invention.